

FIG.1 PRIOR ART

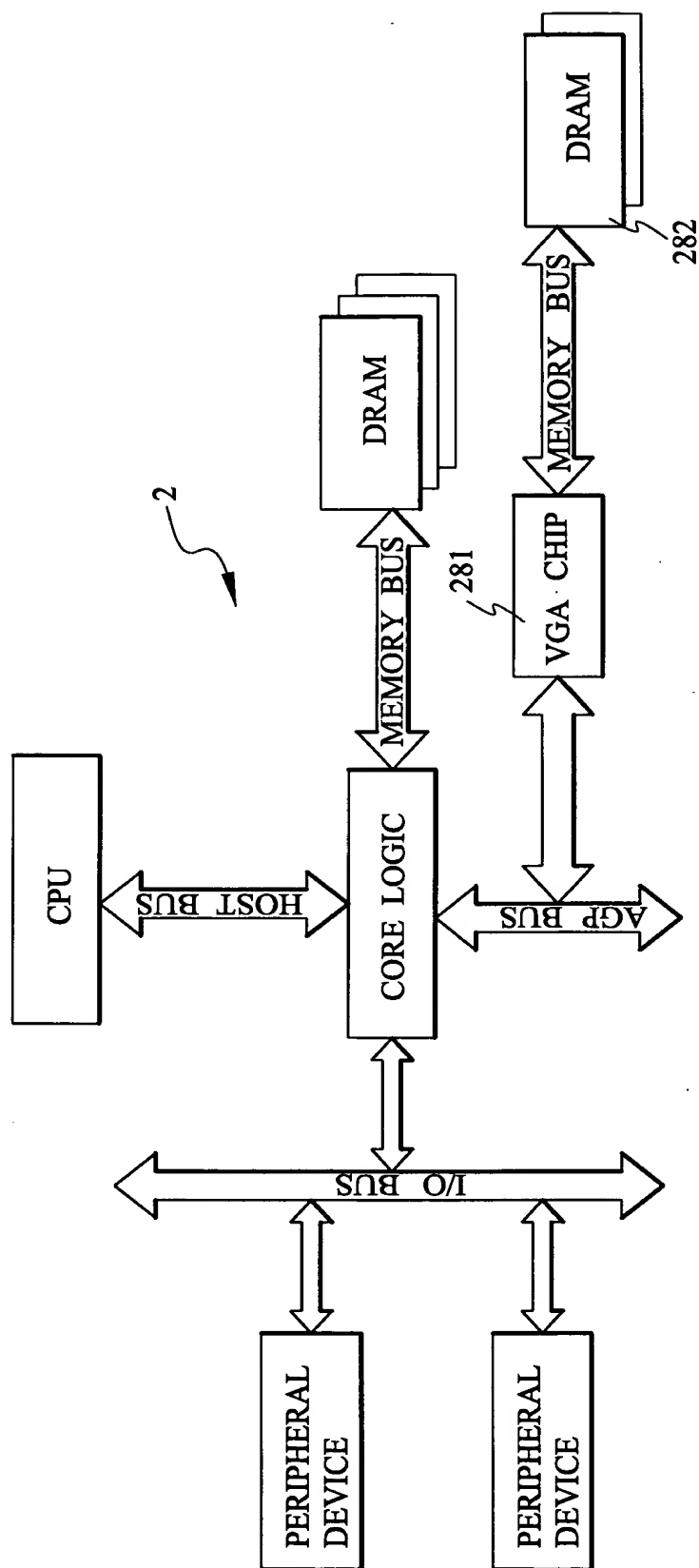


FIG.2 PRIOR ART

FIG. 3 is a block diagram of a system architecture in accordance with the present invention. The system 3 includes a CPU 30, a CORE LOGIC 32, a PERIPHERAL DEVICE 36, a WIRE-OR MEMORY BUS 33, a DRAM 34, a VGA CHIP 38, and an I/O BUS 35. The CPU 30 is connected to the CORE LOGIC 32 via a HOST BUS 31. The CORE LOGIC 32 is connected to the PERIPHERAL DEVICE 36 via the I/O BUS 35. The CORE LOGIC 32 is also connected to the WIRE-OR MEMORY BUS 33, which is connected to the DRAM 34. The CORE LOGIC 32 is further connected to the VGA CHIP 38 via an AGP BUS 37 and a MGMT# signal. The CORE LOGIC 32 is also connected to the I/O BUS 35 via an MREQ# signal.

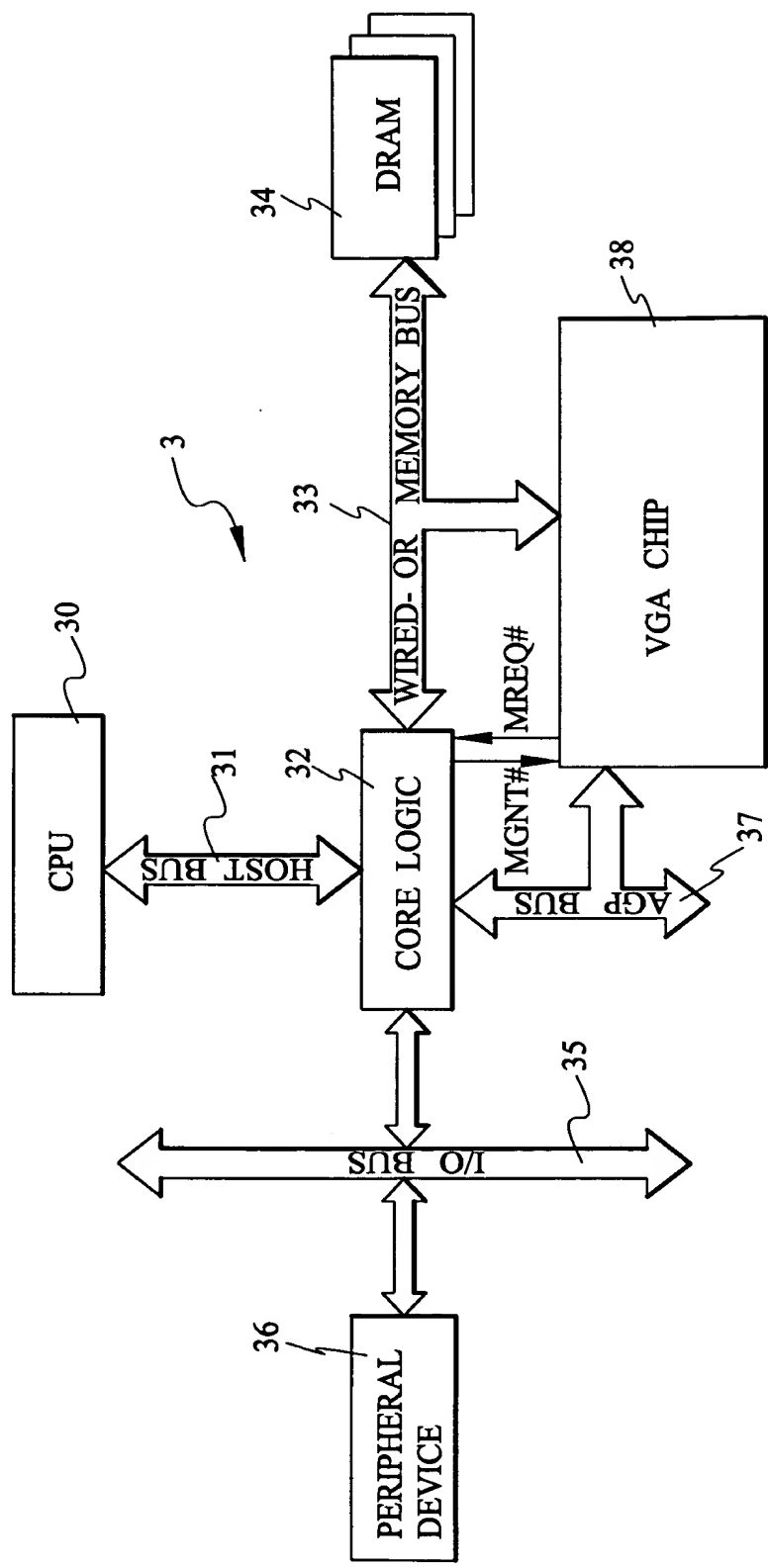


FIG.3 PRIOR ART

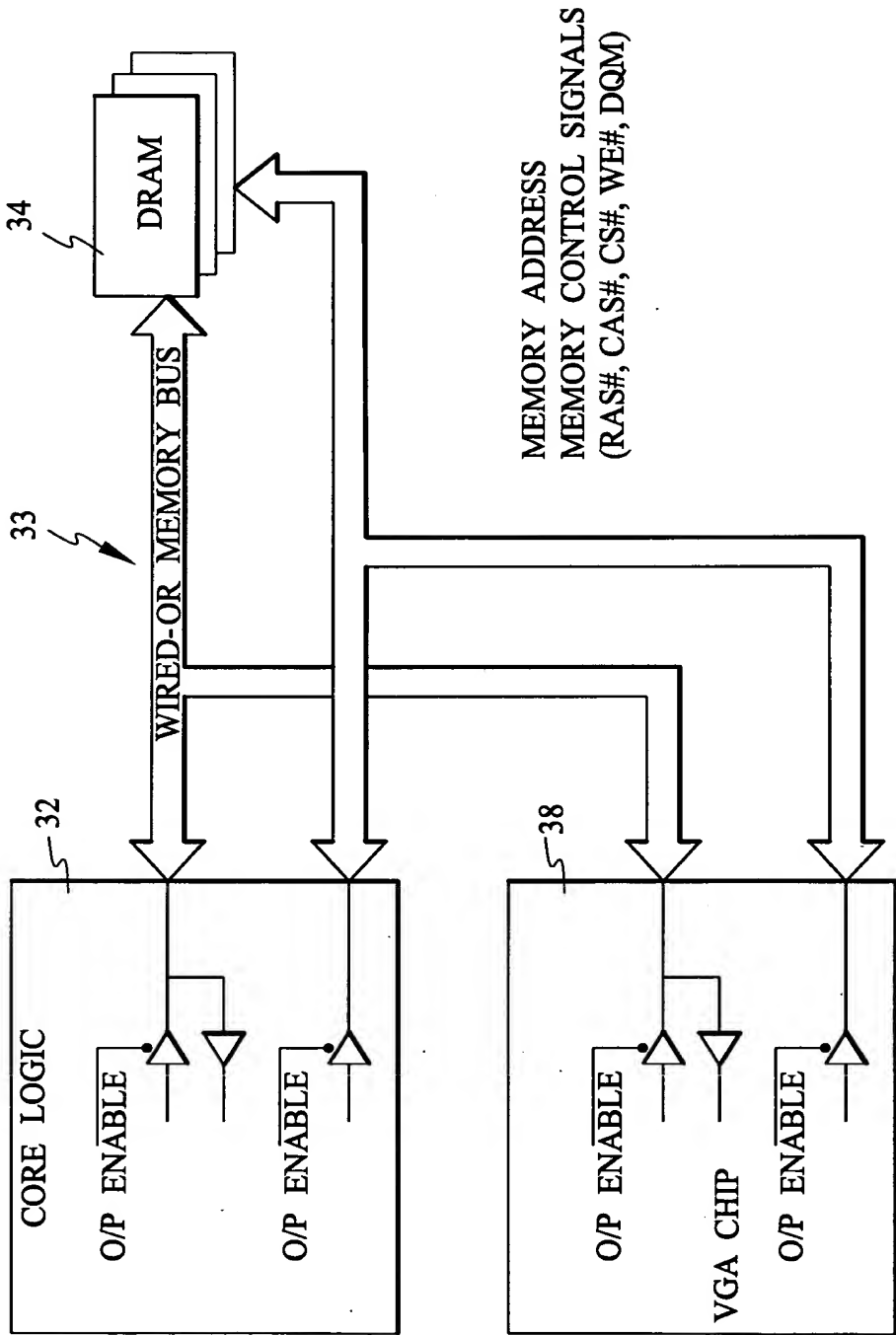


FIG. 4 PRIOR ART

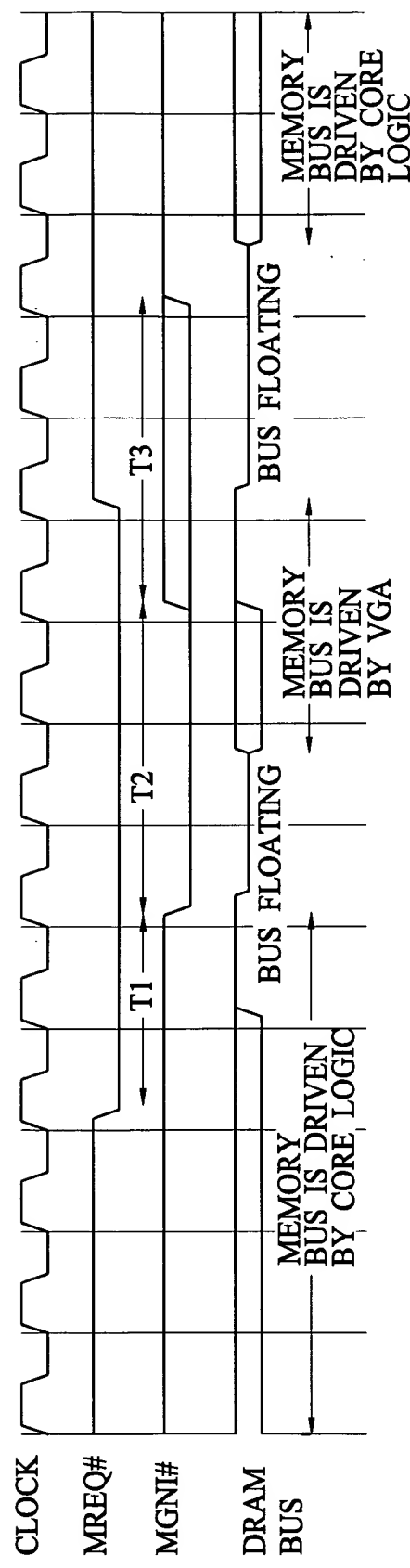


FIG. 5 PRIOR ART

FIG. 6 PRIOR ART

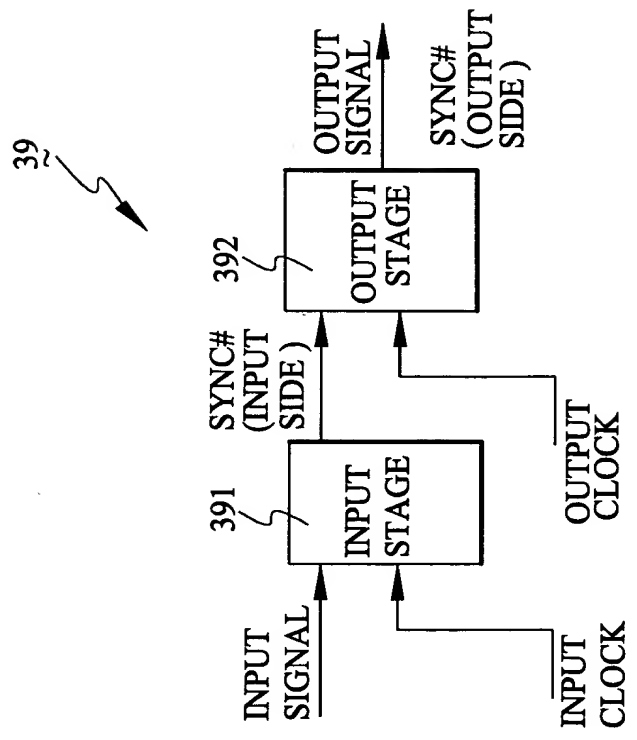


FIG. 6 PRIOR ART

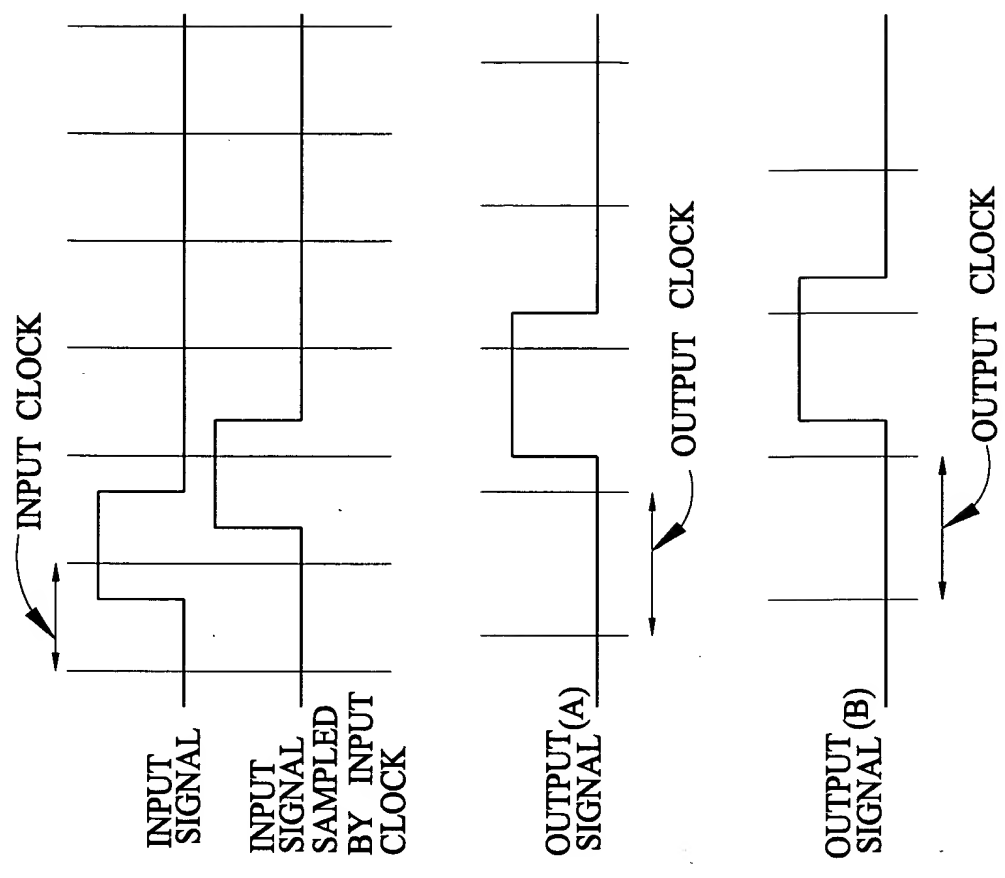


FIG. 7 PRIOR ART

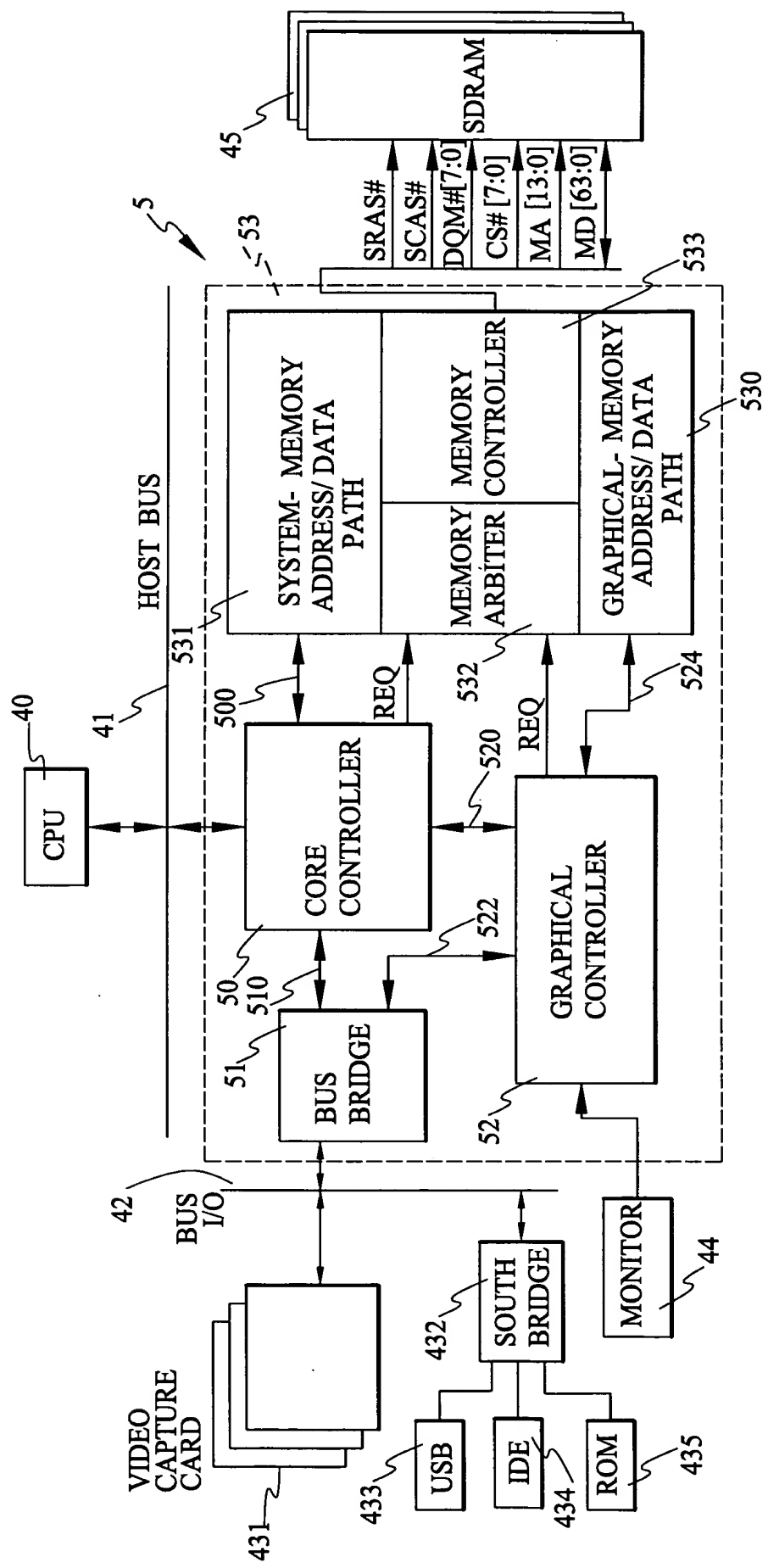


FIG. 8